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Thermal Considerations for High Power and Interplanetary CubeSats

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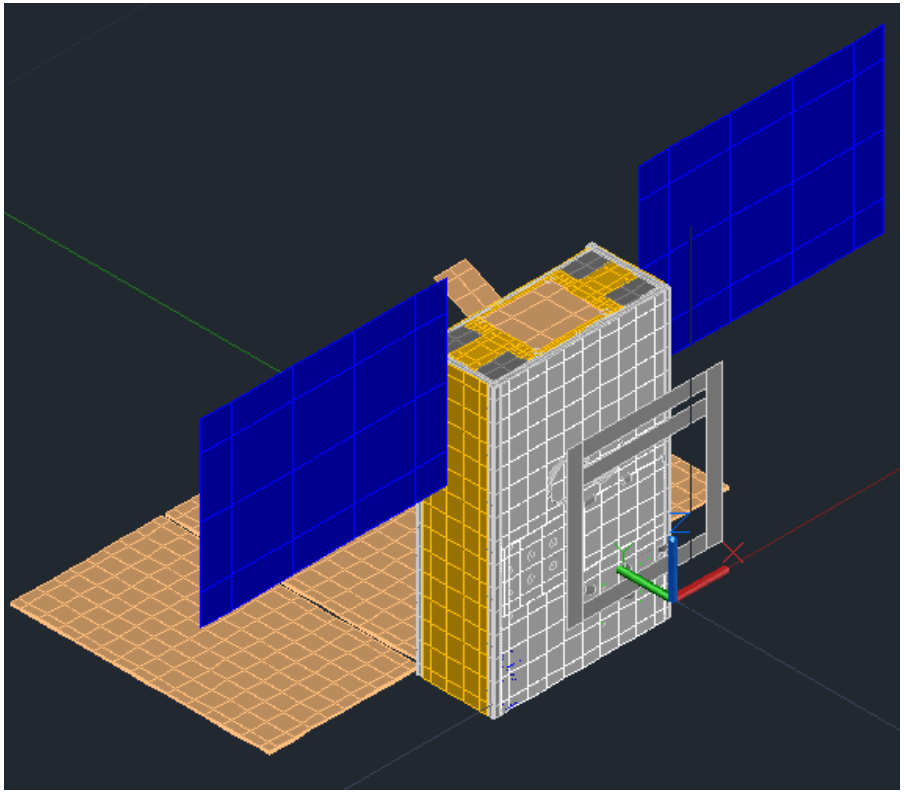
Outline

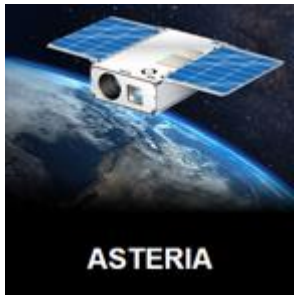
- Background
- Shortcomings of COTS CubeSat Architectures
- Thermal Design Solutions
- Mars-Bound Case Study
- Lessons Learned

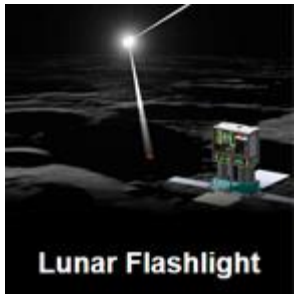


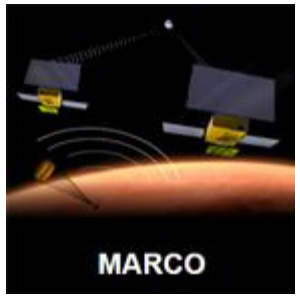
Background

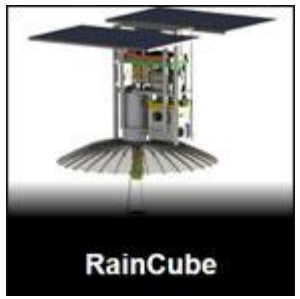
- The capability of CubeSat-class missions has grown substantially since their inception in 2003
  - Asteria - CMOS Imager
  - ISARA - Ka-band Communication
  - Lunar Flashlight - Solar Sail Propulsion
  - MarCO - UHF → X-band Relay
  - NEAScout - Solar Sail Propulsion
  - RainCube - Ka-band Radar

Interplanetary







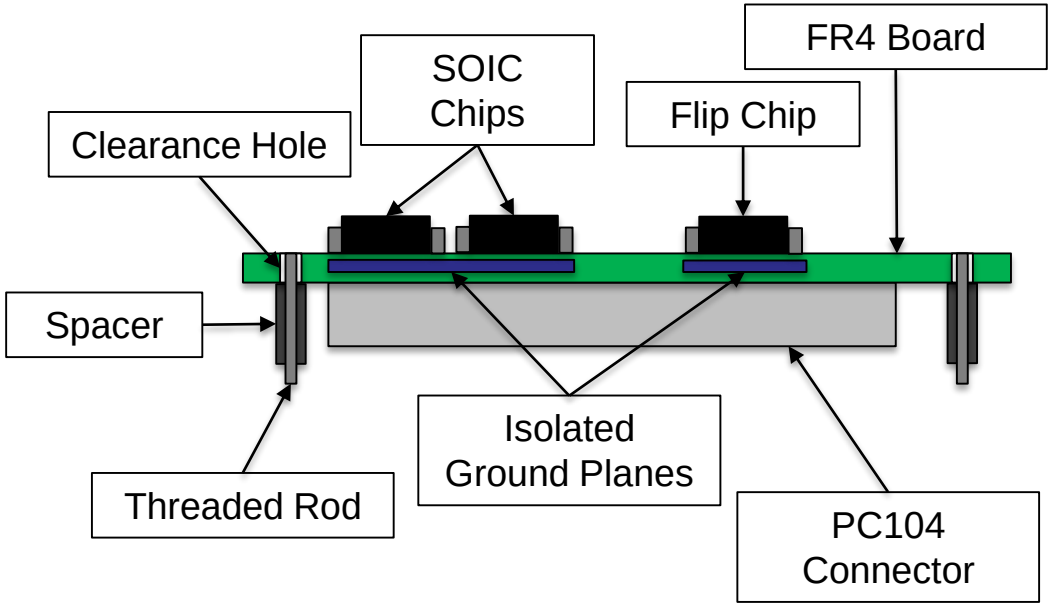


Comparison of Typical CubeSat Mission in 2003 vs. 2015

	2003	2015
Mass (kg)	1	14
Volume (U)	1	6
Power (W)	2	40
Payload	• Active Torque-Rod ACS • Body-Mounted Solar Array (x6) • CMOS Imaging System • GPS Antenna (x2) • GPS Receiver • Li Battery Pack • On-Board Computer (C&DH) • UHF Radio (Rx/Tx) • UHF Antenna (x2)	• Active Reaction Wheel ACS • Deployable Solar Array (x2) • Deployable UHF Antenna • Deployable X-Band Antenna • Deployable X-Band Feed • Cold Gas Microprop System • Command and Data Handling • Electrical Power System • Li Battery Pack • Low-Noise Amplifier • Star Tracker • Solid-State Power Amplifier • UHF Radio (Rx) • X-Band Radio (Rx/Tx)
Destination	Earth	Mars, Moon, Near-Earth Asteroid

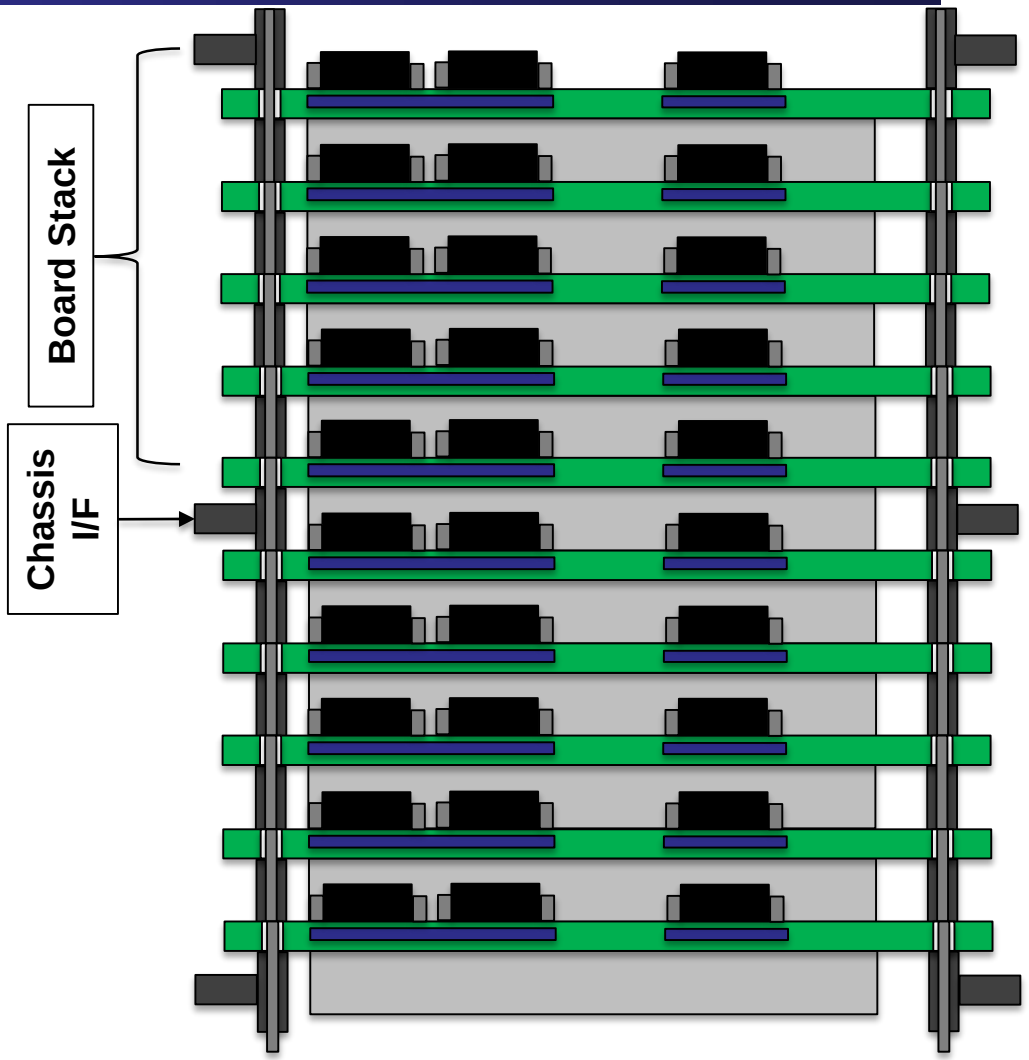
Shortcomings of COTS CubeSat Architectures (Board – Level)

- COTS small outline integrated circuit (SOIC) parts have large internal thermal resistance (~40°C/W Junction-to-Case)
- Boards designed with single point ground in mind
  - Internal copper layers isolated from mechanical I/F
  - Minimal joint pressure at mechanical interface
  - Large conductive resistance throughout
- May need secondary dedicated thermal interfaces for high dissipating components



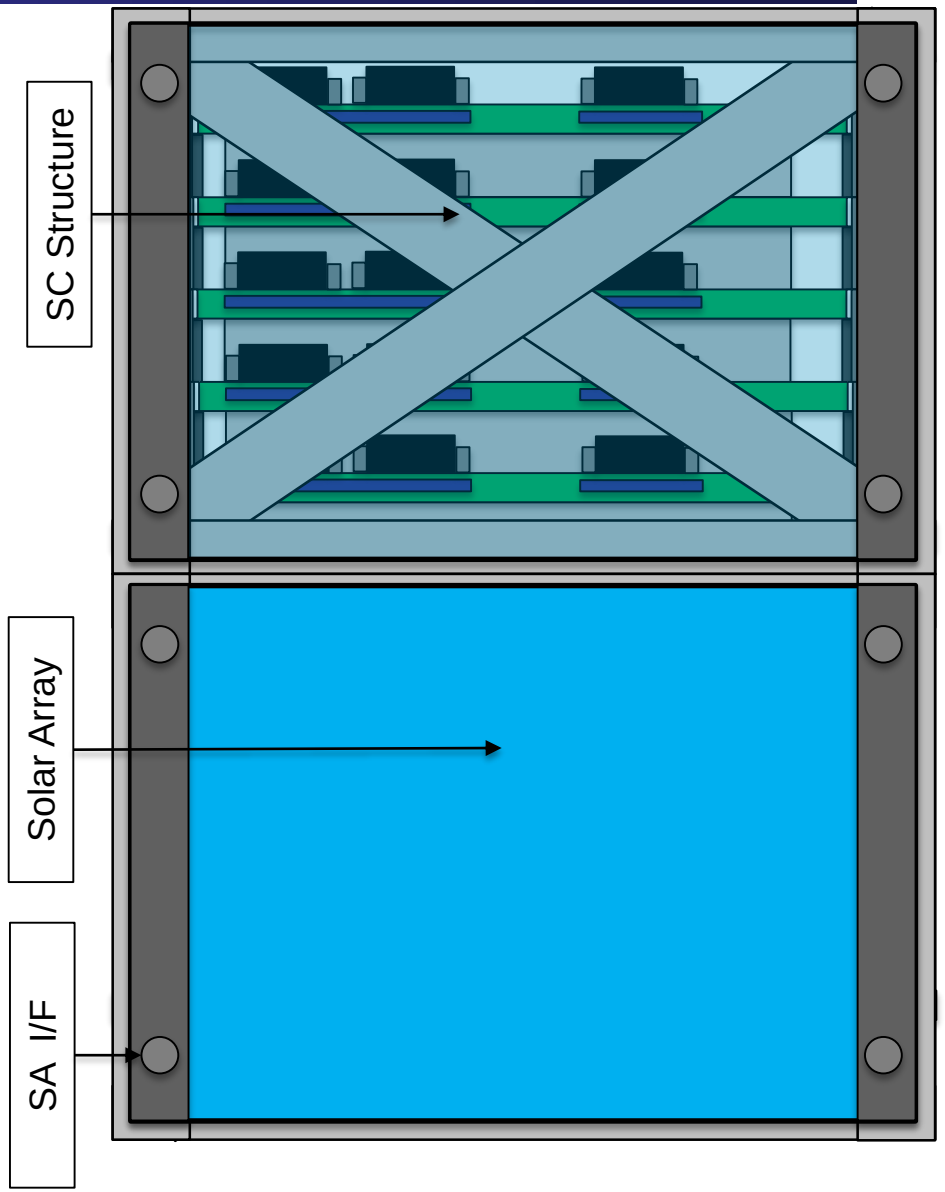
Shortcomings of COTS CubeSat Architectures (Subsys. – Level)

- Board-level mechanical interfaces stacked in series
- Long path length from board power sources to thermal sink
- Limited chassis tie-in locations
  - Exacerbates already poor conductive coupling
  - ΔT rise exponential with board distance to chassis I/F
- Threaded rod to chassis I/F is a clearance hole
- Limits permissible board dissipations > 2-3 W



Shortcomings of COTS CubeSat Architectures (System – Level)

- Lack of dedicated radiators
  - SA is dual-purpose structure
- Body mounted solar cells
  - Adverse loading when $I_{draw} < I_{supply}$
- Large in plane resistance
  - Light-weighted structure
  - Low SA substrate thermal conductivity (FR4)
- Weak SA conductive coupling to chassis
  - 4 x #4-40 per U



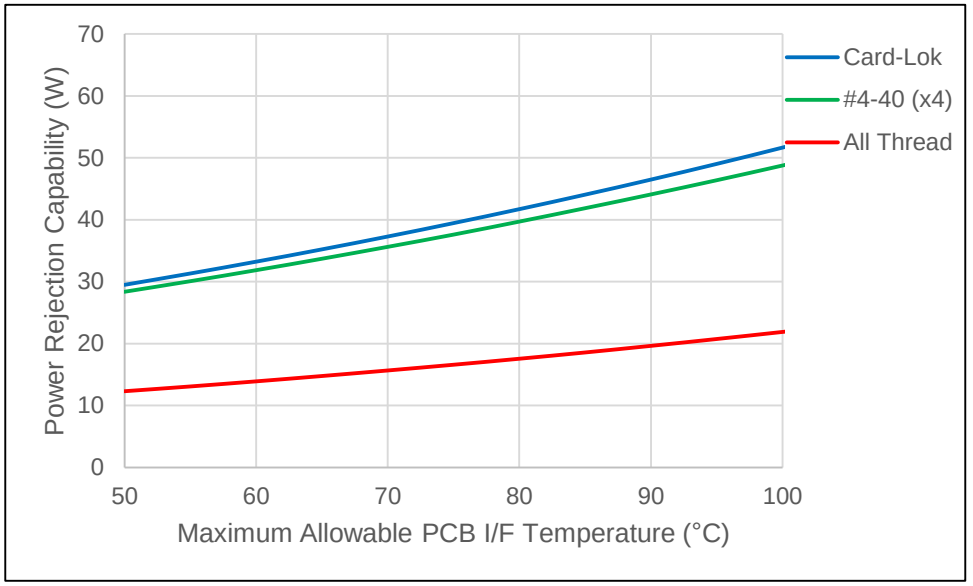
Shortcoming of COTS CubeSat Architectures

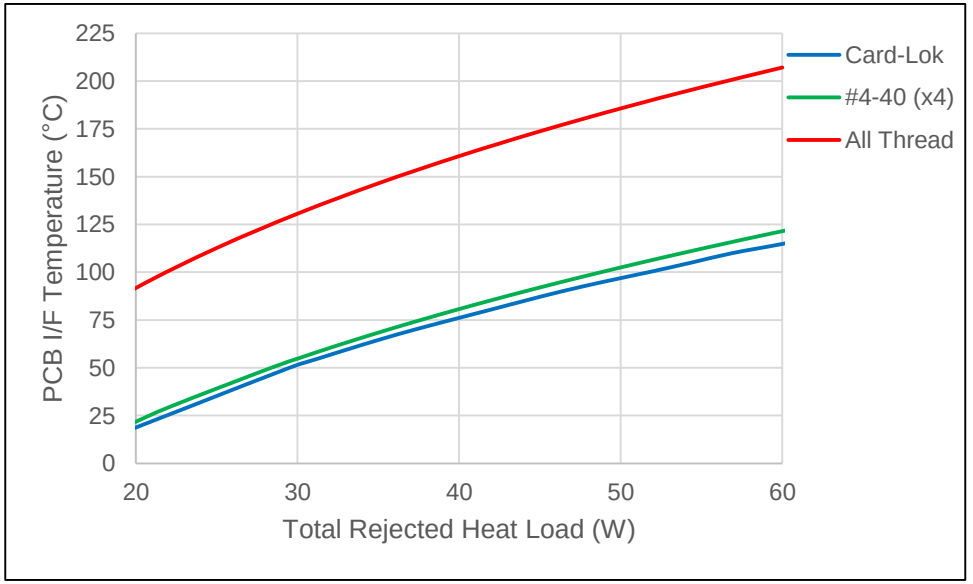
- Thermal design neglected throughout board, subsystem, and system-level assemblies

- Only solutions available to maintain acceptable component temperatures are operational constraints
  - Limits science return

Thermal Design Solutions (Board – Level)

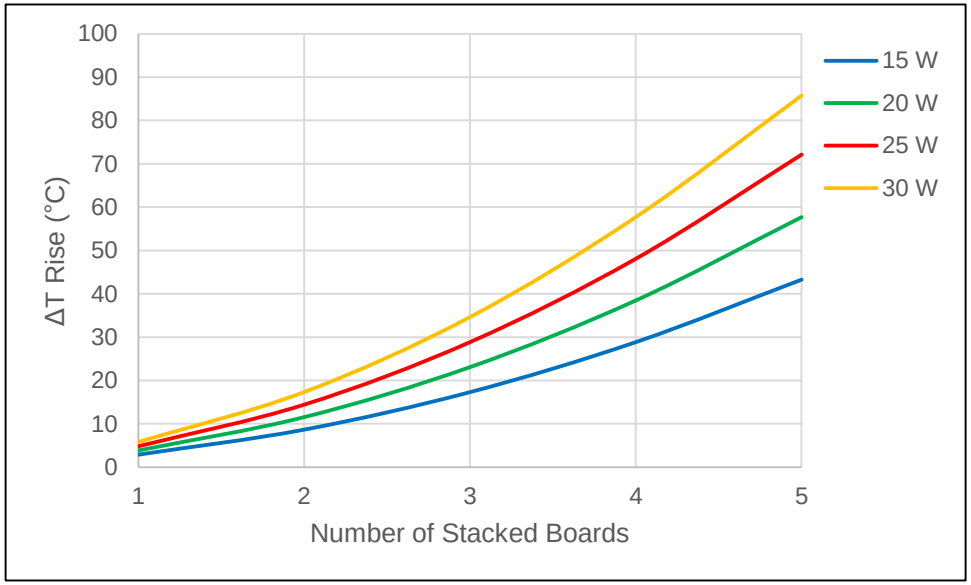
- Limit use of high internal thermal resistance for active components
- Include copper layers that directly interface with mechanical mounting interface
- Provide interfaces for both die-sunk and flip chips (FPGA)
- Card-Lok and #4-40 (x4) possess > 2x power handling capability vs. COTs at given temperature
- Card-Lok and #4-40 (x4) run ~75°C cooler at given power load





Thermal Design Solutions (Subsystem – Level)

- Limit board stacking
  - Limit to 2-3 for modest power applications (15 – 20 W)
  - More may be acceptable for low-power applications



- Discrete mechanical interfaces provide greater power handling capability

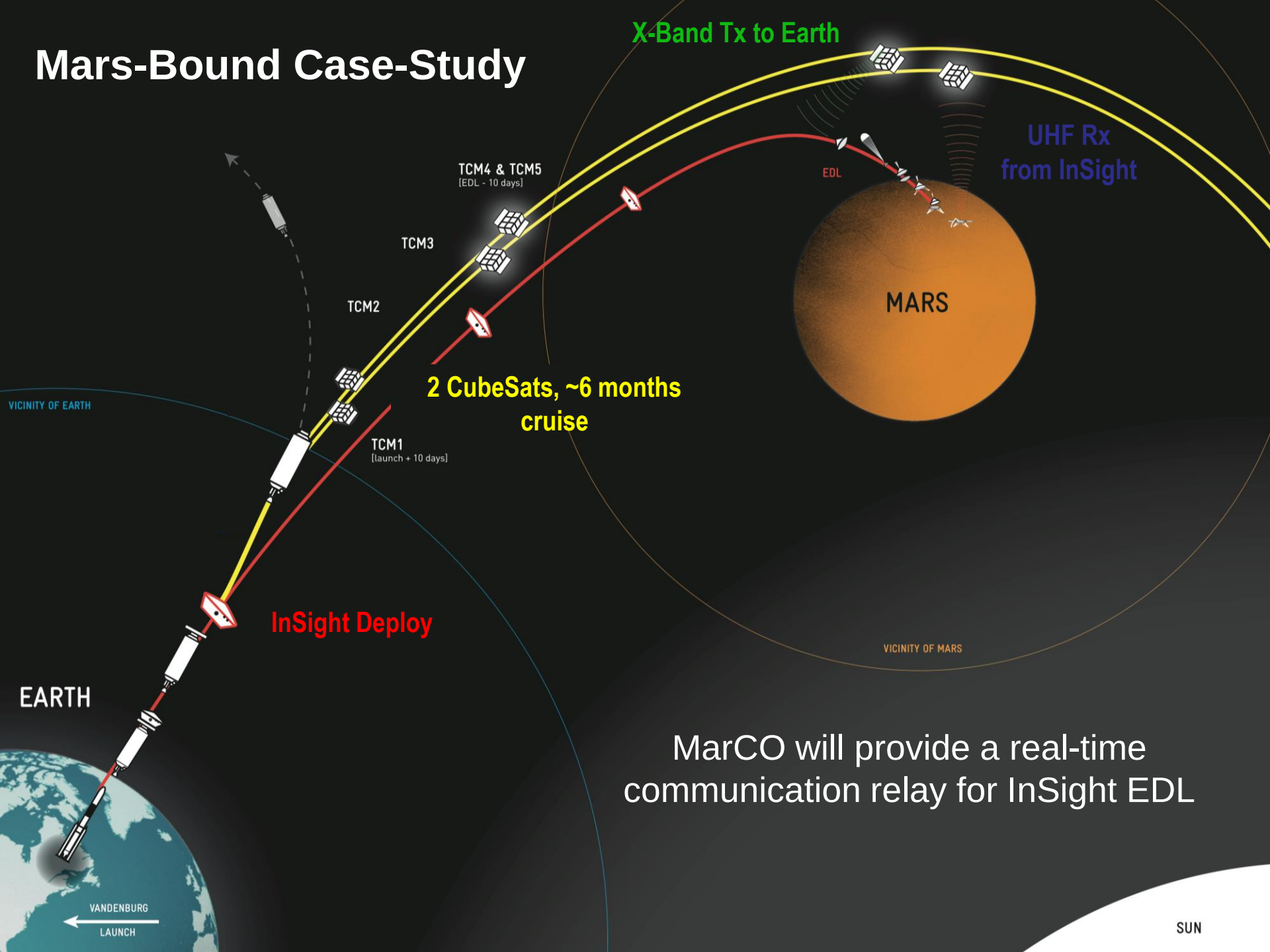
- Must design for lowest common denominator part
  - Commercial = 70°C
  - Industrial = 85°C
  - Military = 125°C

- Plan for lower radiator temperature for stacked configuration to compensate for adverse ΔT

Thermal Design Solutions (System – Level)

- Eliminate use of non-isolated body-mounted solar cells
  - Decreases impact of high absorbed solar flux during charging
- Limit use of light-weighted structures to non-thermal interfaces
  - High-spreading resistance reduces effective radiator area (poor fin efficiency)
- Provide sufficient subsystem – system thermal coupling
  - Use controlled volatile silicone-based gap filler
  - Don’t skimp on the fasteners!
  - Fastener number is for thermal, not mechanical, reasons

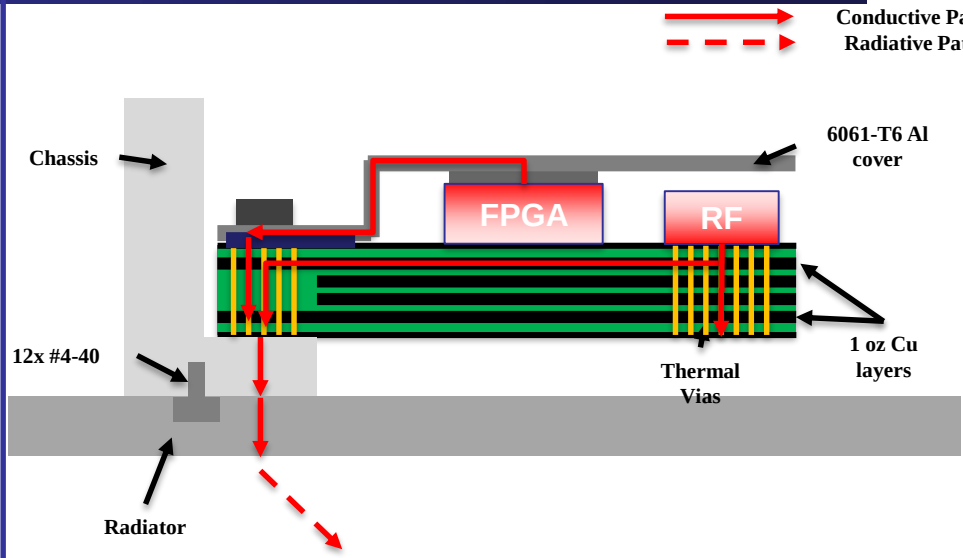
Mars-Bound Case-Study

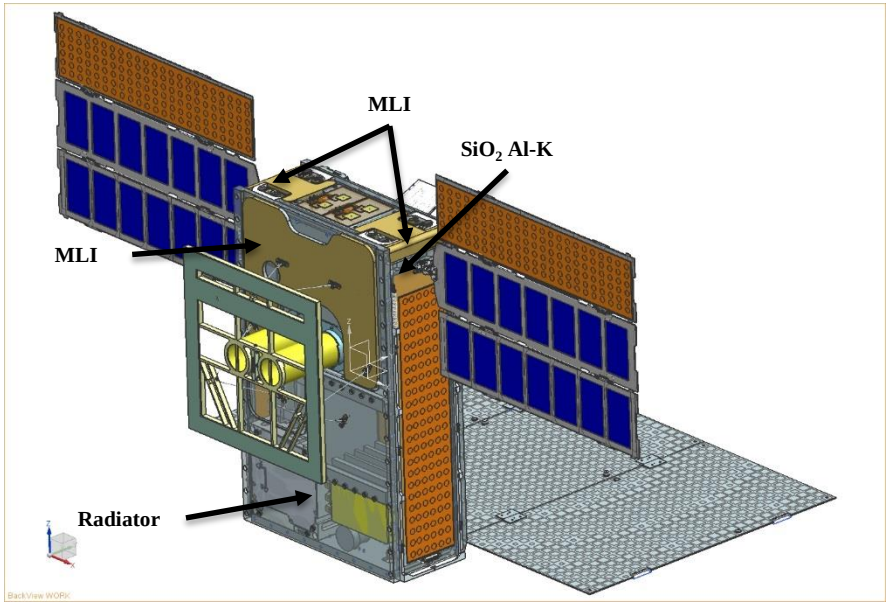


MarCO will provide a real-time communication relay for InSight EDL

Mars-Bound Case Study (MarCO)

- Transponder designed for thermal performance
  - Dedicated thermal PWB Cu layers
  - Custom Al thermal cover for FPGA
  - High conductance chassis
- All active H/W thermally coupled to radiator
  - Minimize ΔT (junction to radiator)
- High mCp interior (~5.2 kg: Electronics & Radiator)
  - Reduces dT/dt during peak power periods





- Designed for low power operation (ΣP_{bus} < 15 W)
- Radiator sized for S.S. -10°C operation at 15 W
  - Capability for ~ 3 hours transmit time
- MLI closeout large non-radiator surfaces
- SiO_2 Al-K closeout on small non-radiator surfaces
  - Reduces solar heat load near Earth
  - Reduces SC heat loss near Mars

Lessons-Learned

- Maintain traceability for critical TMM inputs (P_{diss}, duty cycles, component masses)
  - MEL/PEL tend to overestimate
  - HW CogE less likely to provide credible “will not fall below values”
  - Do the legwork to obtain reasonable estimates vs. carbon copy of MEL/PEL

- Maintain flexibility early on in the design phase
  - Rapidly changing configs, power modes, comp. masses and volumes
  - Implement a simple, robust design to absorb uncertainty
  - Maximize use of simple analyses to down select candidate thermal designs

- Delay detailed model construction until design solidifies
  - Overhead of detailed model early increases analysis turnaround time
  - Wait until higher fidelity will not be achieved until HW in hand